IN THE SPECIFICATION

Please replace the paragraph at page 1, lines 12-17, with the following rewritten paragraph:

The present invention relates to a semiconductor memory including an error correction function by use of an error correction code (ECC) and, more particularly, to[[,]] a semiconductor memory including no resetting functions that [[is]] are used, for example, in a mass-storage SRAM.

Please replace the paragraph beginning at page 1, line 19, to page 2, line 7, with the following rewritten paragraph:

With an improvement in fine patterning and storage capacity of a semiconductor memory, manufacturing technologies have been becoming more sophisticated and difficult to implement, thus making it difficult to manufacture at a high yield such a memory product that all memory cells in the memory operate properly. Further, improved fine patterning has reduced a capacitance to be held in each bit cell, thus causing a phenomenon of random destruction of a one-bit error (which is referred to as [[an]] a soft error) owing to cosmic radiation or alpha radiation to occur frequently to such an extent that it cannot be ignored. This soft error phenomenon cannot be repaired by redundancy technologies and so has been becoming a big problem. As one solution for this problem, a memory has a correction function inside.

Please replace the paragraph beginning at page 2, line 23, to page 3, line 1, with the following rewritten paragraph:

This ECC control circuit comprises a read data register 23, an ECC code register 24, an ECC code generation circuit 25, a syndrome generation circuit 26, an ECC decoding

circuit (syndrome decoder) 27, and a correction data ~~resister~~ register 28, thus having the following basic functions.

Please replace the paragraph beginning at page 5, line 18, to page 6, line 1, with the following rewritten paragraph:

The following will consider a case where a bit width n of the data memory 11 is set larger than a bit width of input/output data of the I/O circuit 10 or [[a]] such a function (mask function) is provided as to write only some bits of input data in the data memory 11. In this case, in order to create an ECC code in first data writing after power application, data needs to be read from the data memory beforehand and referred to, so that it is difficult to avoid the above mistaken correction problem, resulting in writing back an incorrect ECC code.

Please replace the paragraph beginning at page 11, line 23, to page 12, line 7, with the following rewritten paragraph:

The ECC control circuit 13 includes, as shown in FIG. 2 for example, a read data register 23, an ECC code register 24, an ECC code generation circuit 25, a syndrome generation circuit 26, an ECC decoding circuit (syndrome decoder) 27, and a correction data ~~resister~~ register 28. It also includes the same basic functions (1) and (2) as those of the conventional ECC control circuit 13 described above with reference to FIG. 7, and (3) further it can provide control so that error correction may not be conducted for data read from the memory in first data reading after power application, as a function.

Please replace the paragraph at page 13, lines 9-15, with the following rewritten paragraph:

(2) In ordinary data reading, the same operation as in the above data reading before ordinary data writing is performed. In this case, data stored in the read data register 23 passes through the correction data ~~resister~~ register 28 as it is or is corrected one bit at the correction data ~~resister~~ register 28, to provide output data.

Please replace the paragraph beginning at page 15, line 22, to page 16, line 9, with the following rewritten paragraph:

~~To the~~ The one pair of bit lines BL and /BL is further connected to an initialization releasing circuit 33. This initialization releasing circuit 33 is constituted of a third clocked inverter circuit IV3 connected between the ground node and the other bit line (second bit line) /BL, a fourth clocked inverter circuit IV4 connected between the one pair of bit lines BL and /BL, a NOR circuit NOR for taking a negated logical sum of three inputs of a bit line pre-charge signal, Bprech, a potential of the second bit line /BL, and the resetting pulse signal, reset, and inverter ~~circuit~~ circuits IV5 and IV6 which are connected in two stages for buffering and amplifying an output signal (ECC function stop signal: ECC-disable) of this NOR circuit NOR to thereby drive the third and fourth clocked inverters IV3 and IV4.